Amendments to the Specification

Please replace the original title on page 1, line 2, with the following replacement title.

FLOATING BODY CELL DYNAMIC RANDOM ACCESS MEMORY WITH OPTIMIZED BODY GEOMETRY ~~SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE~~

Please replace the paragraph at page 1, lines 17-24 as follows:

Semiconductor storage devices including DRAMs are more and more down-scaled in recent years. 1T-1C (1 transistor-1 capacitor) type DRAMs, however, need a certain area for capacitors to secure the storage capacitance of the capacitors. Therefore, 1T-1C DRAMs ~~has~~ have a scaling limitation. Further, since 1T-1C DRAMs need capacitors, their manufacturing process is complicated, increasing their manufacturing cost.

Please replace the paragraph at page 1, lines 25-31 as follows:

To cope with this problem, techniques for forming DRAMs on ~~a~~ an SOI (silicon on insulator) substrate have been developed. For example, Japanese Patent Laid Open Publication No. JP-2002-246571 (herein below referred to as Patent Document 1) discloses a DRAM comprising FBCs (Floating Body Cells). The FBC is a memory cell composed of one transistor using ~~a~~ an SOI substrate.

Please replace the paragraph at page 1, lines 32-36 as follows:

The FBC is formed as a MOS transistor on ~~a~~ an SOI substrate. Its SOI layer includes a source region, drain region and body region. The body region confined between the source region and the drain region is electrically floating.

Please replace the paragraph at page 2, lines 1-12 as follows:

The drain current varies with the number of holes in the body region. Data "1" and data "0" can be distinguished by the grade of change of the drain current. That is, by controlling the number of holes accumulated in the body region, the FBC can store data. For example, when more holes exist in the body region, the FBC identifies the data as "1". When fewer holes exist in the body region, the FBC identifies the data as "0". In this type of the FBC, in general, the larger the capacitance between the body region and a fixed potential element such as a support substrate, the data ~~hold~~ retention time is longer, and the function yield is better.

Please replace the paragraph at page 2, lines 13-16 as follows:

The FBC described in Patent Document 1 increases the capacitance between the body region and the support substrate by using ~~a~~ an SOI substrate having a thin buried oxide film (herein below referred as BOX layer).

Please replace the paragraph at page 2, lines 24-29 as follows:

Therefore, the larger the better the capacitance between the body region and the support substrate in the region where an FBC is formed whereas the smaller the better the parasitic capacitance between the SOI layer region and the support substrate in the region where peripheral circuits and logic circuits are formed.

Please replace the paragraph at page 2, line 32 through page 3, line 14 as follows:

A semiconductor device of an embodiment according to the invention comprises a semiconductor substrate; a first insulation layer formed on the semiconductor substrate; a

semiconductor layer insulated from the semiconductor substrate by the insulation layer; a source region of a first conduction type and a drain region of the first conduction type formed in the semiconductor layer; a body region of a second conduction type formed in the semiconductor layer between the source region and the drain region, said body region being capable of storing data by accumulating or releasing electric charge; a second insulation layer formed on the body region; a word line formed on the second insulation layer and insulated from the body region by the second insulation layer; and a bit line electrically connected to the drain region, wherein the area of the body region in contact with the ~~second~~ first insulation layer is larger than the area thereof in contact with the ~~first~~ second insulation layer.

Please replace the paragraph at page 4, lines 17-35 as follows:

A method of manufacturing a semiconductor device of an embodiment according to the invention comprises: preparing ~~a~~ an SOI substrate having a semiconductor layer insulated from a support substrate by a first insulation layer; forming a mask material on the semiconductor layer; patterning the mask material; etching the semiconductor layer in accordance with the mask material and thereby partly exposing the first insulation layer; implanting an impurity into the support substrate in an energy level permitting the impurity to penetrate the exposed part of the first insulation layer but not permitting the same to penetrate the mask material; forming a third insulation layer between adjacent portions of the semiconductor layer; removing the mask material; forming a gate insulating layer on the semiconductor layer; forming a gate electrode on the gate insulating layer; and forming a source region and a drain region in the portions of the semiconductor layer at ~~opposite~~ both sides of the gate electrode.

Please replace the paragraph at page 4, line 36 through page 5, line 20 as follows:

A method of manufacturing a semiconductor device of a further embodiment according to the invention comprises: preparing ~~a~~ an SOI substrate having a semiconductor layer insulated from a support substrate by a first insulation layer; forming a mask material on the semiconductor layer; patterning the mask material; etching an upper lying part of the semiconductor layer in accordance with the mask material while maintaining the remainder lower part of the semiconductor layer; forming a spacer on side surfaces of the mask material and on side surfaces of the upper lying part of the semiconductor layer; etching the semiconductor layer by using the mask material and the spacer as a mask, and thereby partly exposing the first insulation layer; forming a third insulation layer between adjacent portions of the semiconductor layer; removing the mask material; forming a gate insulating layer on the semiconductor layer; forming a gate electrode on the gate insulating layer; and forming a source region and a drain region in the portions of the semiconductor layer at ~~opposite~~ both sides of the gate electrode.

Please replace the description at page 5, lines 30-31 as follows:

Fig. 4 is a graph showing body potentials when data ~~id~~ is "1" and "0";

Please replace the paragraph at page 7, line 27 through page 8, line 4 as follows:

Fig. 2 is a cross-sectional view of a unit cell U taken along the A-A line of Fig. 1. Fig. 3A is a cross-sectional view of the unit cell U taken along the B-B line of Fig. 1, and Fig. 3B is a cross-sectional view of a peripheral logic circuit. First referring to Fig. 2, the DRAM 100 further includes a BOX layer 120, an SOI layer 130, and a p^+ type semiconductor substrate having impurity concentration equal to or higher than 10^{19} cm^{-3}~~, BOX layer 120 and SOI layer 130~~. The BOX layer lies on the semiconductor substrate 110 and electrically insulates the SOI layer 130 from the semiconductor substrate 110. The semiconductor substrate 110 and the SOI

layer 130 may be composed of single-crystalline silicon ~~silicon single crystal~~, and the BOX layer l20 may be made of SiO_2, for example.

Please replace the paragraph at page 8, lines 5-23 as follows:

The SOI layer 130 includes n-type source regions 132, n-type drain regions 134, and p-type body regions 136 each located between a source region 132 and a drain region 134. A gate insulating film 140 is provided on the body region 136, and word lines WL [[is]] are provided on the gate insulating film 140. The gate insulating film 140 is made of SiO_2, for example. The word lines WL are insulated from the body regions 136 by the gate insulating film 140. Referring to Fig. 3A, STI (Shallow Trench Isolation) 170 is formed to confine the body regions 136 from front and back directions. The STI 170 is made of SiO_2 for example. As a result, the body regions 136 are each enclosed by the insulating material and the semiconductor material different in conduction type, and the body regions 136 are therefore held electrically floating. Thus, the potential of each body region 136 may vary depending upon the potentials of the semiconductor substrate 110, word line WL, source region 132 and drain region 134.

Please replace the paragraph at page 8, lines 24-27 as follows:

Thickness of [[he]] the BOX layer 120 is one to five times the thickness of the gate insulating film 140. If the thickness of the gate insulating film 140 is 5 nm, thickness of the BOX layer 120 will be 5 nm to 25 nm.

Please replace the paragraph at page 9, lines 28-35 as follows:

In addition, since the impurity concentration at the boundary between the semiconductor substrate 110 and the BOX layer 120 in the DRAM region is not lower than

$10^{19}cm^{-3}$, the instant embodiment does not permit a depletion layer in the semiconductor substrate 110, or can diminish the thickness of the depletion layer. Therefore, the embodiment can raise the capacitance value Csub more than conventional techniques.

Please replace the paragraph at page 10, lines 24-32 as follows:

The body region 136 can store data by accumulating or discharging electric charges. For example, the word line WL and the bit line BL are set in relatively high potentials, and the FBC is biased to its saturated state. As a result, impact ionization occurs in the body region 136, and holes are accumulated in the body region 136. Thereby, data "1" is written in the FBC. ~~Let the data "1" be stored when~~ The data state is designated as "1" when more holes are accumulated in the body region 136.

Please replace the paragraph at page 10, line 33 through page 11, line 4 as follows:

On the other hand, when the bit line BL is set in a relatively low potential and the word line WL is set in a relatively high potential, a pn junction between p-type body region 136 and n-type drain region 134 is biased forward. In this case, the holes heretofore accumulated in the body region 136 are discharged to the bit line BL through the drain region 134. As a result, data "0" is written in the FBC.

Please replace the paragraph at page 12, lines 1-14 as follows:

As shown in Fig. 4, in the conventional DRAM 10, the body potential difference d_0 between data "1" and data "0" at the time t1 decreases to the potential difference d_{10} at the time t3. In the DRAM 100 according to the instant embodiment, the body potential difference d_0 decreases to the potential difference d_{100} at the time t3. The potential difference d_{100} in the DRAM 100 according to the instant embodiment is larger than the potential difference d_{10} in

the conventional DRAM 10. In general, a larger difference between V1 and V0 allows easier distinction between data "1" and data "0", and enhances the function yield. Therefore, DRAM 100 is easier to distinguish data "1" from data ~~"02~~ "0" than the conventional DRAM 10, and assures a better production yield.

Please replace the paragraph at page 13, lines 8-17 as follows:

If the ratio of contribution of Cd to the body region is large, when the bit line BL is returned to the hold state (t1~t2), the body potential difference (V1-V0) between data "1" and data "0" largely decreases. For example, when the bit line BL decreases from 1.5 volt to 0 volt, V1 decreases by 1.5V*(Cd/(Csub+Cd+Cs+Cg), and V0 increases by 1.5V*(Cd/(Csub+Cd+Cs+Cg)). From these equations, it is ~~appreciated~~ expected that the body potential difference (V1-V0) increases when the SOI is formed thinner and Cd is reduced accordingly.

Please replace the paragraph at page 13, lines 18-31 as follows:

If the ratio of contribution of Cg to the body region is large, ~~then the word line WL is returned to the hold state (t2~t3), potential difference between data "1" and data "0" largely decreases~~ potential difference between data "1" and data "0" largely decreases when the word line WL is returned to the hold state (t2~t3). In this case, for example, V1 becomes lower than V0 by as much as 1.5V*(Cg/(Csub+Cd+Cs+Cg)). This is because the transistor varies in threshold voltage as much as 1.5 volt between data "1" and data "0", and the degree of the capacitance coupling between the word line WL and the body region 136 therefore varies as much as 1.5 volt. Further, from those equations, it is ~~appreciated~~ expected that the body potential difference (V1-V0) increases as the capacitance between the word line WL and the body region decreases.

Please replace the paragraph at page 14, line 32 through page 15, line 6 as follows:

As shown in Fig. 5, first prepared is an SOI substrate including a semiconductor substrate 110, BOX layer 120 and SOI layer 130. The top surface of the SOI layer 130 is oxidized to form a silicon oxide film 201. Thickness of the BOX layer 120 is approximately 25 nm.

Please replace the paragraph at page 16, lines 5-19 as follows:

Fig. 7B is a cross-sectional view of the peripheral logic circuit in this step. In the region of the peripheral logic circuit, no spacers preferably exist. For this purpose, after the spacer is once formed in both the DRAM region and the peripheral logic circuit region, a photolithographic step and an etching step are added. That is, while the DRAM region is covered by photo resist, the spacer in the region of the peripheral logic circuit is removed by etching. As a result, the device region in the peripheral logic circuit region is ~~etched by using~~ patterned using the silicon nitride film 203 as a mask as shown in Fig. 7B, and no steps ST are formed therein. In this process, injection of high-concentrated impurity ions into the semiconductor substrate 110 in the peripheral logic circuit region ~~is avoided~~ is not performed so as not to increase the parasitic capacitance.

Please replace the paragraph at page 17, line 28 through page 18, line 1 as follows:

After that, an ~~isolating~~ insulation film is deposited on the silicide layers 160, 162, 164 ~~to form plugs electrically connected to the silicide layer 164 and the poly silicon plug 152 in the isolating insulation film~~ followed by formation of plugs in the insulation film electrically connected to the silicide layer 164 and the poly silicon plug 152. In addition, bit lines BL are formed on the plugs to intersect with the word lines WL approximately at a right angle. The bit

lines BL may be a metal such as copper, aluminum or tungsten, for example. Through these steps, the DRAM 100 shown in Figs. 1 through 3B is completed.

Please replace the paragraph at page 18, line 24 through page 19, line 3 as follows:

In contrast, the instant embodiment executed ion injection into the semiconductor substrate 110 after the etching of the SOI layer 130 as shown in Fig. 7A. Therefore, no impurities are injected to the SOI layer 130, and the surface of the semiconductor substrate 110 can be doped with a sufficiently high concentration of impurity to thereby increase the capacitance value Csub. Injection of the impurity into the SOI layer 130 in the instant embodiment can be attained in the same manner as the conventional technique. Therefore, impurity concentration of the semiconductor substrate 110 and impurity concentration of the SOI layer 130 can be determined independently from each other. Therefore, it is possible to design a memory cell enhanced in body potential difference (V1-V0) and elongated in data ~~hold~~ retention time.

Please replace the paragraph at page 20, line 12 through page 21, line 3 as follows:

Additionally, another manufacturing method of DRAM 300 is explained. This method is identical to the manufacturing method of DRAM 100 up to the step of anisotropic etching of the upper part of the SOI layer 130 while maintaining the lower part thereof in Fig. 6. Next formed is a photo resist having the pattern PR (see Fig. 17) in the DRAM region and fully open in the peripheral logic circuit. After that, the SOI layer 130 is selectively etched by using the photo resist and the silicon nitride film 203 as a mask. As a result, the BOX layer in the STI regions near the drain regions of the DRAM 300 and the BOX layer 120 in the STI regions in the peripheral logic circuit region are exposed. Thereafter, a spacer material is deposited on the substrate. Then, a photo resist fully opened in the DRAM region is formed, and the spacer

material is selectively removed by anisotropic etching by RIE or the like to obtain the spacer 250 (Fig. 7). Then, using the silicon nitride film 203 and the spacer 250 as a mask, the SOI layer 130 is selectively removed by RIE to expose the BOX layer 120 of the STI regions in the DRAM region. Thus, step portions ST corresponding to the thickness of the spacer 250 are formed in the body regions 136 and the source regions 132 (see Fig. 1) only in the DRAM region. After the spacer 250 is removed, the same steps as those of the first embodiment (see Figs. 8 through 12) may be conducted. ~~DRAM 300 can be manufactured also by the method explained here~~ As explained above, DRAM 300 can be manufactured.

Please replace the paragraph at page 21, lines 4-26 as follows:

As shown in Fig. 17, distance D between ~~en~~ an edge of each word line WL and an edge of a pattern PR in the DRAM 300 may be ~~made~~ adjustable appropriately. For example, step portions ST near the n-type drain regions may be fully removed by reducing the distance D to zero. In this case, the area of the PN junction between each n-type drain region and each p-type body region is smaller than that of the DRAM 100. As a result, because the value of Cd is smaller than that of the DRAM 100, distinction between data "1" and data "0" is easier in the DRAM 300 than in DRAM 100. Therefore, DRAM 300 is better in function yield and can hold data for a longer time. Furthermore, in the DRAM 300, although the value of Cd is approximately equal to that of the conventional DRAM 10, values of Csub and Cs are larger. The body potential difference (V1-V0) after the word line WL returns to its hold state can be expressed as approximately 1.5V*((Csub+Cs-Cd)/(Csub+Cd+Cs+Cg)). As compared with the first embodiment where Cd=Cs, DRAM 300 according to this embodiment exhibits a larger value of Cs than Cd, and this effect also contributes to easier distinction between data "1" and data "0", better function yield and longer data ~~hold~~ retention time.

Please replace the paragraph at page 28, lines 2-19 as follows:

A semiconductor device includes ~~comprises~~ a semiconductor substrate; a first insulation layer formed on the semiconductor substrate; a semiconductor layer insulated from the semiconductor substrate by the insulation layer; a source region of a first conduction type and a drain region of the first conduction type formed in the semiconductor layer; a body region of a second conduction type formed in the semiconductor layer between the source region and the drain region, said body region being capable of storing data by accumulating or releasing electric charge; a second insulation layer formed on the body region; a word line formed on the second insulation layer and insulated from the body region by the second insulation layer; and a bit line electrically connected to the drain region, wherein the area of the body region in contact with the first ~~second~~ insulation layer is larger than the area thereof in contact with the second ~~first~~ insulation layer.